06-23-00

PTO/SB/05 (2/98)

Please type a plus sign (+) inside this box → [+]

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	TI-29276
First Named Inventor or Application Identifier	Francis G. Celii
Title	PROCESS FLOW FOR DUAL DAMESCENE INTERCONNECT STRUCTURES
Express Mail Label No.	EL356820115US

On Page 1 of the specification, before line 1, insert –This application claims priority under 35 USC § 119(e)(1) of provisional application number **60/143,282** filed **07/12/99**.--

APPLICATION ELEMENTS

See MPEP Chapter 600 concerning utility patent application contents

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] *Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification *[Total Pages* [12] *]* *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R&D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC d113)* *[Total Sheets* [6] *]*
4. Oath or Declaration *[Total Pages* [3] *]*
   - a. [X] Newly Executed (orginal or copy)
   - b. [ ] Copy from a prior application (37 CFR §1.63(d)) *(for continuation/divisional with Box 17 completed)*

   [Note Box 5 below]

   - i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR §1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)* The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   - a. [ ] Computer Readable Copy
   - b. [ ] Paper Copy (identical to computer copy)
   - c. [ ] Statement verifying identical of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & Documents(s))
9. [ ] 37 CFR §3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
14. [ ] *Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
15. [ ] Certified Copy of Priority Document(s) *if foreign priority is claimed)*
16. [ ] Other:

*A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon

17. If a CONTINUING APPLICATION, *check appropriate box and supply the requisite information below and in a preliminary amendment:*

☐Continuation ☐Divisional ☐Continuation-in-part (CIP) of prior application No: / .

Prior application information: ***Examiner*** _____ ***Group / Art Unit:*** _____

18. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

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Name (Print/Type)	Jacqueline J. Garner	Registration No. (Attorney/Agent)	36,144
Signature		Date	6/22/00

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

	Celii et al.	Examiner:	TBD
Serial No:	TBD	Art Unit:	TBD
Filed:	6/22/00	Docket No.:	TI-29276
For:	PROCESS FLOW FOR DUAL DAMESCENE INTERCONNECT STRUCTURES		

PRELIMINARY AMENDMENT

June 15, 2000

Assistant Commissioner for Patents

Washington, DC 20231

Dear Sir:

Please amend the above referenced application as follows:

In the Specification:

Page 1, before line 1, insert --This application claims priority under 35 USC § 119(e)(1) of provisional application numbers **60/143,282** filed **07/12/99**.--

REMARKS

Entry of the foregoing amendment prior to examination is respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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Attorney for Applicants
Reg. No. 36,144

PROCESS FLOW FOR DUAL DAMESCENE INTERCONNECT STRUCTURES

FIELD OF THE INVENTION

The invention is generally related to the field of forming interconnect structures in a semiconductor device and more specifically to a dual damascene process flow for forming interconnect structures.

BACKGROUND OF THE INVENTION

As the density of semiconductor devices increases, the demands on interconnect layers for connecting the semiconductor devices to each other also increases. Therefore, there is a desire to switch from the traditional aluminum metal interconnects to copper interconnects. Unfortunately, suitable copper etches for a semiconductor fabrication environment are not readily available. To overcome the copper etch problem, damascene processes have been developed.

In a damascene process, the IMD is formed first. The IMD is then patterned and etched to form a trench for the interconnect line. If connection vias have not already been formed, a dual damascene process may be used. In a dual damascene process, after the trench is formed in the IMD, a via is etched in the ILD for connection to lower interconnect levels. The barrier layer 14 and a copper seed layer are then deposited over the structure. The barrier layer 14 is typically tantalum nitride or some other binary transition metal nitride. The copper layer is the formed using the seed layer over the entire structure. The copper is then chemically-mechanically polished (CMP'd) to remove the copper from over the IMD 16, leaving copper interconnect lines 18 and vias 20 as shown in FIG. 1. A metal etch is thereby avoided.

Further improvements in interconnect performance are desired. Accordingly, efforts are being made to include low-k dielectric materials in a copper interconnect structure.

SUMMARY OF THE INVENTION

The invention is a dual damascene process flow for forming interconnect lines and vias in which at least part of the via is etched prior to the trench etch. A low-k material such as a thermoset organic polymer is used for the ILD. The IMD may comprise the same material, another low-k material, or a slightly higher-k material. After the at least partial via etch, a BARC is deposited over the structure including in the via. Then, the trench is patterned and etched. Although at least some of the BARC material is removed during the trench etch, the bottom of the via is protected.

An advantage of the invention is providing a dual damascene process flow compatible with a low-k material.

This and other advantages will be apparent to those of ordinary skill in the art having reference to the specification in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIG. 1 is a cross-sectional diagram of a prior art dual damascene interconnect structure;

FIGs. 2A-2K are cross-sectional diagrams of a dual damascene process flow according to a first embodiment of the invention;

FIGs. 3A-3B are cross-sectional diagrams of a dual damascene process flow according to a second embodiment of the invention;

FIGs. 4A-4B are cross-sectional diagrams of a dual damascene process flow according to a third embodiment of the invention; and

FIG. 5 is a cross-section diagram of a test structure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

The invention will now be described in conjunction with a copper interconnect/thermoset organic polymer dielectric dual damascene process flow. It will be apparent to those of ordinary skill in the art that the benefits of the invention are applicable to other dual damascene process flows including those for metals other than copper and dielectrics other than thermoset organic polymers.

A first embodiment of the invention is described in conjunction with FIG. 2A-2K. A semiconductor body 100 is processed through the formation of a first interconnect level 102. First interconnect level 102 may in fact be Metal 1 or it may be any metal interconnect level other than the upper most interconnect layer. A passivation layer 104 is formed over first interconnect level 102. In the preferred embodiment passivation layer 104 comprises silicon nitride. Alternative materials for passivation layer 104 include, but are not limited to, SiC or variants with SiN, such as SiN:C. For example, BloK™ from Applied Materials may be used.

ILD 106 is deposited over passivation layer 104. ILD 106 preferably comprises a low-k material such as an organic polymer. In the preferred embodiment, ILD 106 comprises SiLK™. SiLK™ is a thermoset organic polymer manufactured by Dow Chemical Company. SiLK™ has attractive materials properties for IMD/ILD applications, including a dielectric constant of k = 2.65, as measured by MOS capacitors, high thermal stability (Td > 450° C), and a glass transition temperature that is at or above the maximum SiLK™ curing temperature. SiLK™ includes aromatic functional groups and oxygen atoms. Characterization of SiLK™ films by FT-IR spectroscopy does not reveal highly polarizable functionalities such as carbonyl groups.

If SiLK™ is used, it may be deposited by spin coating and furnace annealing. A thickness nonuniformity of less than 5% (1σ). To improve the adhesion of SiLK™ to silicon dioxide and silicon nitride, an adhesion promoter may be spun-on the wafer prior to SiLK™ deposition. The adhesion promoter may be comprised of silicon, oxygen, carbon, and hydrogen atoms. The adhesion promoter may have a thickness on the order of 100Å.

A shelf layer 108 is formed over ILD 106 followed by deposition of IMD 110. The composition of shelf layer 108 is such that IMD 110 may be etched selectively with respect to shelf layer 108. A selectivity on the order of 20:1 or greater is desirable. IMD 110 may also comprise a low-k material such as an organic polymer. Alternatively, IMD 110 may comprise a slightly higher–k dielectric material (higher than ILD 106 but still less than or equal to that of silicon dioxide). In the preferred embodiment, IMD 110 comprises SiLK™. If SiLK™ is used for IMD 110 and ILD 106, silicon dioxide may be used for shelf layer 108.

In order to pattern and etch a via, a hardmask 112 is formed over IMD 110. Then, a via pattern 114 is formed over hardmask 112. Via pattern 114 typically comprises a resist material. The thickness desired depends on the thickness of ILD 106, IMD 110 and the various etch selectivities. For example, the thickness may be on the order of 6600Å for a ILD thickness of 3900Å, a hardmask thickness of 1550Å and a IMD thickness of 3900Å.

Next, the hardmask 112 is opened in the areas exposed by via pattern 114, as shown in FIG. 2B. An etch chemistry with good selectivity between the hardmask 112 and both the resist pattern 112 and the IMD 110 material is desired. For example, a $Ar/CF_4/O_2/C_2H_4/N_2$ chemistry may be used.

Referring to FIG. 2C, a partial via 116 is etched through IMD 110. If SiLK™ is used, the etch chemistry can comprise $N_2/C_2H_4/O_2$. At least approximately 1:1 selectivity between the resist pattern 112 and IMD 110 material is desired. 2:1 or greater is preferred.

The shelf layer 108 is then opened in via 116 as shown in FIG. 2D. An $Ar/CF_4/O_2/C_2H_4/N_2$ etch chemistry may be used for this etch. Finally, the via 116 is etched through ILD 106, as shown in FIG. 2E. For this etch, a good selectivity between the ILD 106 material and both passivation layer 102 and hardmask 112 is desired. Selectivity against etching hardmask 112 is desired because at this point most and maybe all of the resist pattern 112 may have been removed. Accordingly, a $N_2/O_2/ C_2H_4$, (where HC is a hydrocarbon) etch chemistry may be used.

Referring to FIG. 2F, a layer of BARC (bottom antireflective coating) 120 is deposited over the structure, including in vias 116. A trench pattern 112 is then formed. FIG. 2F shows a slight mis-alignment of trench pattern 112 to illustrate the invention's tolerance for mis-alignment errors. BARC layer 120 comprises a material compatible with photolithography for forming trench pattern 112 and that preferably etches somewhat slower than the low-k material of ILD 106 and etches significantly faster during the subsequent trench etch than passivation layer 104. BARC layer 120 has a thickness on the order of 800Å over IMD 110. The thickness of BARC layer 120 within via 116 is significantly thicker. The thickness of BARC layer 120 is determined by etch selectivities, via aspect ratio, and ILD 106 thickness. It is desired to have some portion of the BARC layer 120 remain in via 116 after the subsequent trench etch. The portion of BARC layer 120 within via 116 must withstand the subsequent BARC etch, hardmask etch, and IMD etch.

Referring to FIG. 2G, the BARC layer 120 and hardmask 112 are etched using pattern 122. As an example, a gas chemistry of Ar/O_2 may be used for the BARC layer 120 and a $Ar/CO/CF_4/C_4F_8$ etch chemistry may be used to open the hardmask.

Referring to FIG. 2H, a trench 124 is etched in IMD 110. A $N_2/O_2/C_2H_4$ chemistry may be used. BARC 120 protects the bottom of via 116 during this etch. The trench etch has a selectivity of approximately 30:1 between the IMD 110 and the passivation layer 104. Passivation layer 104 cannot withstand the entire trench etch process. However, if all BARC material is removed during the trench etch, passivation layer 104 offers some limited protection of the bottom of the via 116.

Preferably, after the trench etch, some BARC material remains with in via 116 protecting the bottom of via 116. The remaining BARC material 120 is removed as shown in FIG. 2I. Then, passivation layer 104 is etched at the bottom of via 116 exposing a portion of the metal in interconnect layer 102.

Finally, the desired barrier layers and copper fill are formed and CMP'd back to form second interconnect layer 126, as shown in FIG. 2K. For example, a TaN barrier may be deposited in trench 124 and via 116 followed by a copper seed layer. Using an electroplating process, the copper fill layer is formed. Then, the copper is chemically-mechanically polished until it is planar with the top of IMD 110 or hardmask 112. The above process may then be repeated to form additional metal interconnect layers.

A second embodiment of the invention is described in conjunction with FIGs. 3A-3B. Semiconductor body 100 is processed as in the first embodiment through the partial via etch shown in FIG. 2C. This approach is a half-via first approach. After half the via 116 is etched (e.g., through the IMD 110), the BARC

layer 120 is deposited and the trench pattern 122 is formed, as shown in FIG. 3A. The hardmask 112 may be etched using a $Ar/CF_4/O_2/C_2H_4/N_2$ chemistry and the via 116 in SiLK™ IMD 110 may be etched using a N_2/O_2/HC chemistry.

With trench pattern 122 in place, the shelf oxide 108 is opened up. The etch chemistry will also remove any BARC 120 material in via 116 prior to opening up the shelf oxide 108.

Next, the trench 124 is etched in IMD 110. Because, the shelf layer 108 was previously removed in via 116, portions of ILD 106 are exposed to this etch. Thus, via 116 is extended through ILD 106, as shown in FIG. 3B. The desired barrier and copper material are then deposited and CMP'd to form second interconnect layer 126 as shown in FIG. 2K.

A third embodiment of the invention is described in conjunction with FIGs. 4A-4B. Semiconductor body 100 is processed as in the first embodiment through the opening of the shelf layer shown in FIG. 2D. This approach is also a half-via first approach. After half the via 116 is etched (e.g., through the IMD 110) and the shelf layer 108 in via 116 is removed, the BARC layer 120 is deposited and the trench pattern 122 is formed, as shown in FIG. 4A. The hardmask 112 may be etched using a $Ar/CF_4/O_2/C_2H_4/N_2$ chemistry and the via 116 in SiLK™ IMD 110 may be etched using a $N_2/O_2/C_2H_4$ chemistry. A chemistry comprising Ar/O_2 may be used to open up the shelf layer 108.

Next, the trench 124 is etched in IMD 110. A N_2/O_2/HCchemistry may be used. The BARC material 120 in via 116 at the beginning of this etch delays the etching of via 116 into ILD 106. Via 116 is still extended through ILD 106 by the end of this etch, as shown in FIG. 4B. However, the delay caused by BARC material 120 prevent punchthrough of the passivation layer 102 at the bottom of

via 116. The desired barrier and copper material are then deposited and CMP'd to form second interconnect layer 126 as shown in FIG. 2K.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.

IN THE CLAIMS:

1. A method of fabricating an integrated circuit, comprising the steps of:

forming an interlevel dielectric layer over a semiconductor body;

forming an intrametal dielectric layer over said interlevel dielectric layer;

forming a hardmask over said intrametal dielectric layer;

forming a via pattern over said hardmask;

selectively etching a via through said hardmask;

extending said via by selectively etching said intrametal dielectric layer;

depositing a BARC layer over said hardmask and within said via;

forming a trench pattern over said BARC layer; and

etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via.

2. The method of claim 1, further comprising the steps of forming a shelf layer between said interlevel dielectric layer and said intrametal dielectric layer; and extending said via by selectively etching through said shelf layer using said via pattern after said etching a via step.

3. The method of claim 2, further comprising the step of extending said via by selectively etching through said interlevel dielectric layer after said step of etching said shelf layer and prior to depositing said BARC layer.

4. The method of claim 3, wherein said depositing a BARC layer step fills said via to a level approximately even with a height of said interlevel dielectric.

5. The method of claim 3, further comprising the step of removing a remaining portion of said BARC layer after said etching a trench step.

6. The method of claim 1, further comprising the step of filling said trench and via with copper.

7. The method of claim 1, wherein said intrametal dielectric layer comprises an organic polymer.

8. The method of claim 1, wherein said intrametal dielectric layer and said interlevel dielectric layer comprise SiLK™.

9. The method of claim 1, wherein said interlevel dielectric comprises an organic polymer.

ABSTRACT

A dual damascene process flow for forming interconnect lines and vias in which at least part of the via (116) is etched prior to the trench etch. A low-k material such as a thermoset organic polymer is used for the ILD (106) and IMD (110). After the at least partial via etch, a BARC (120) is deposited over the structure including in the via (116). Then, the trench (126) is patterned and etched. Although at least some of the BARC (120) material is removed during the trench etch, the bottom of the via (116) is protected.

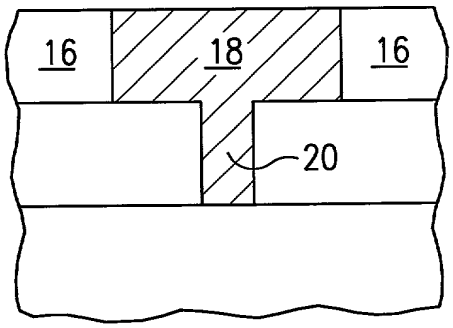

FIG. 1
(PRIOR ART)

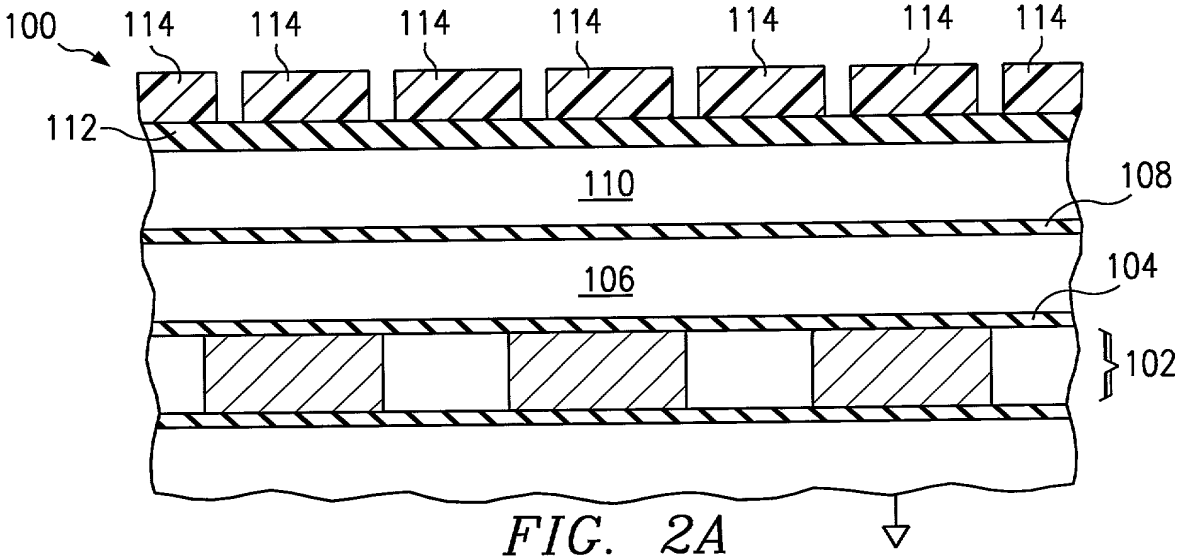

FIG. 2A

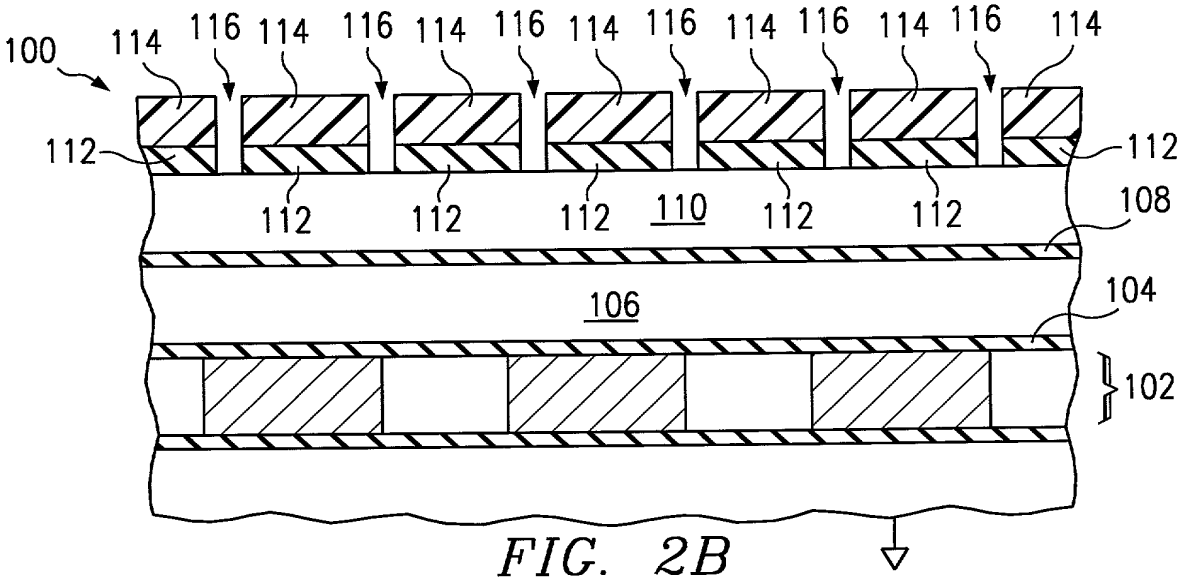

FIG. 2B

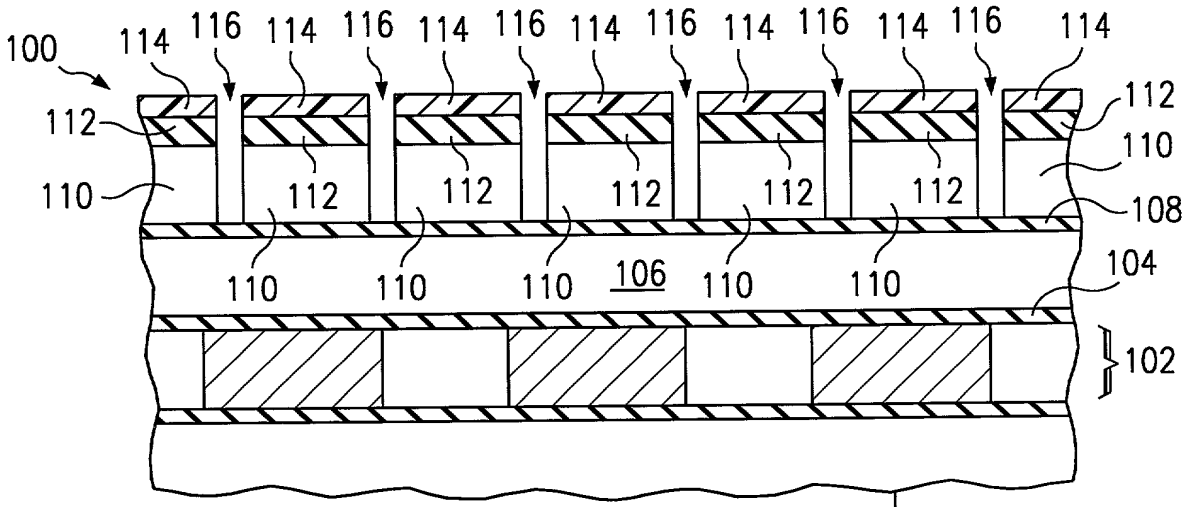

FIG. 2C

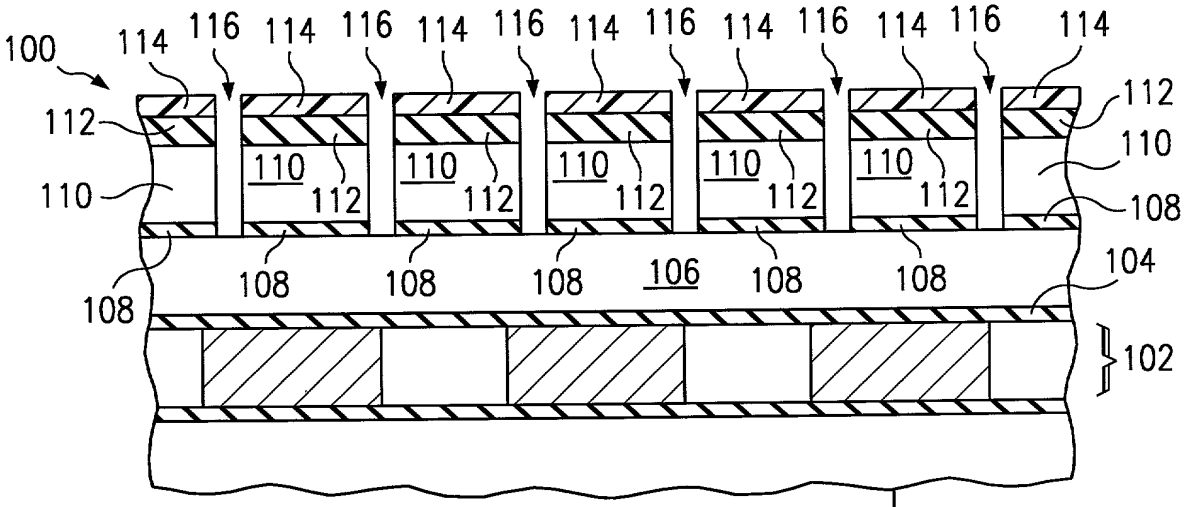

FIG. 2D

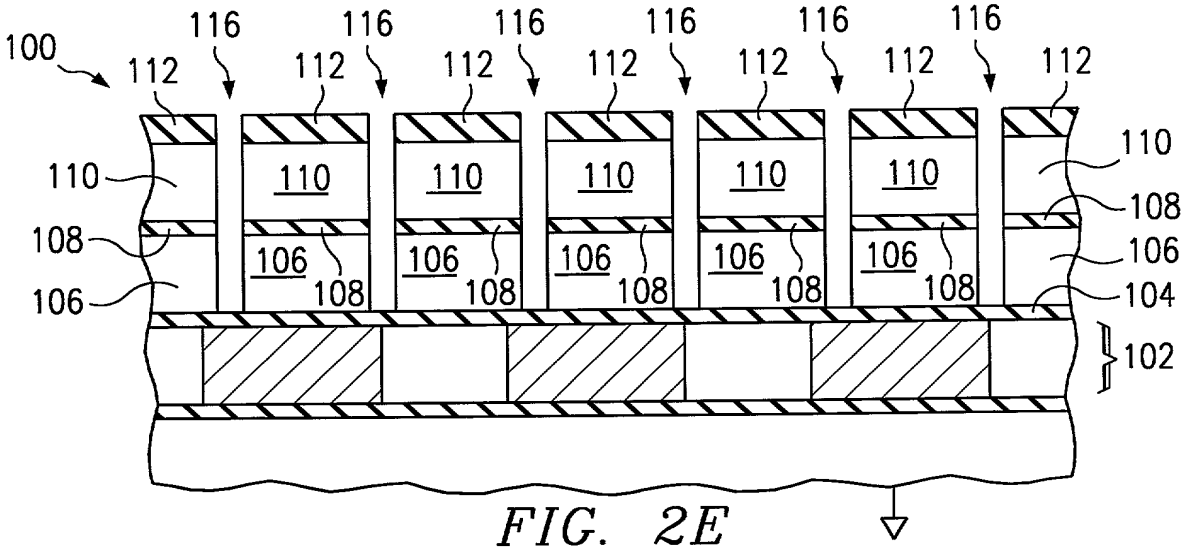

FIG. 2E

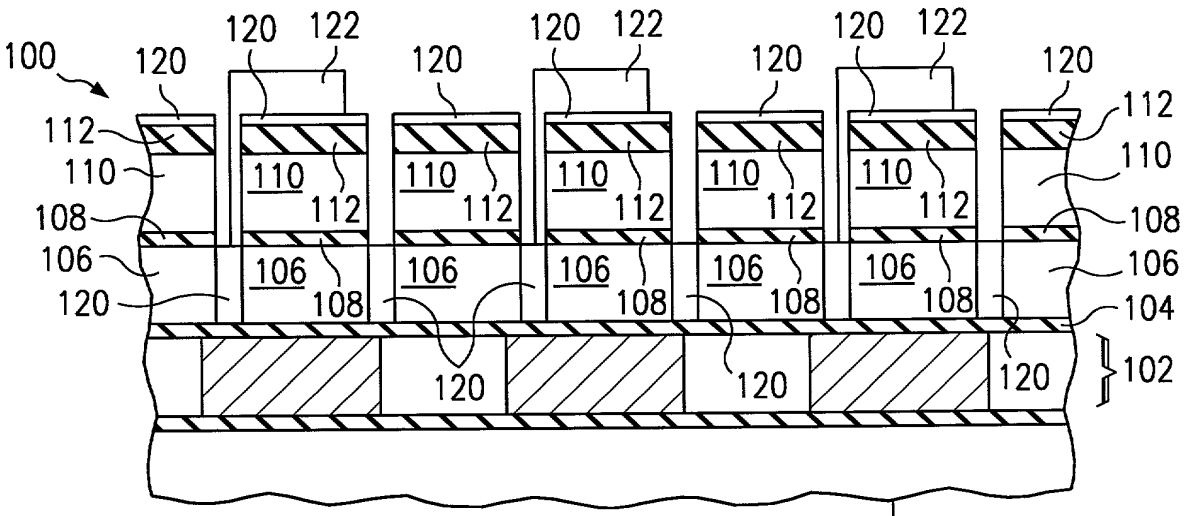

FIG. 2F

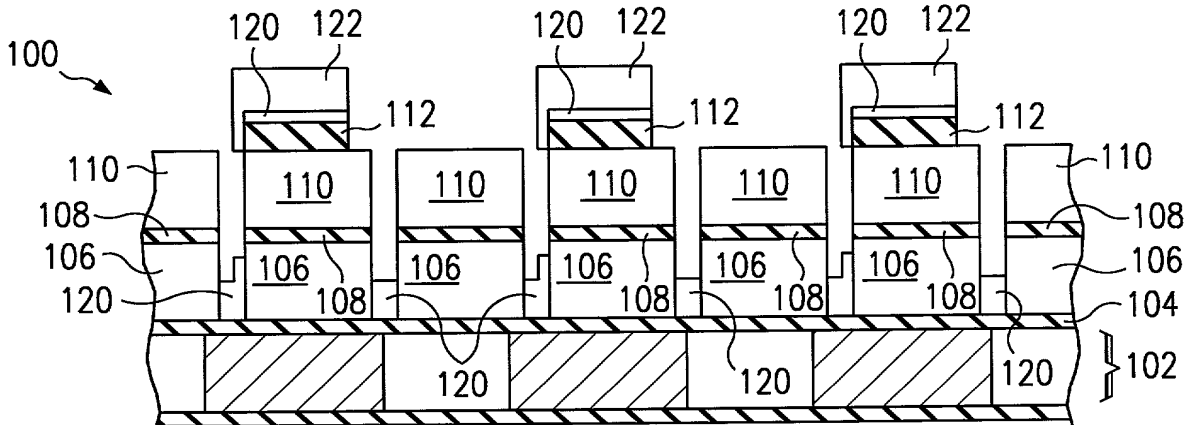

FIG. 2G

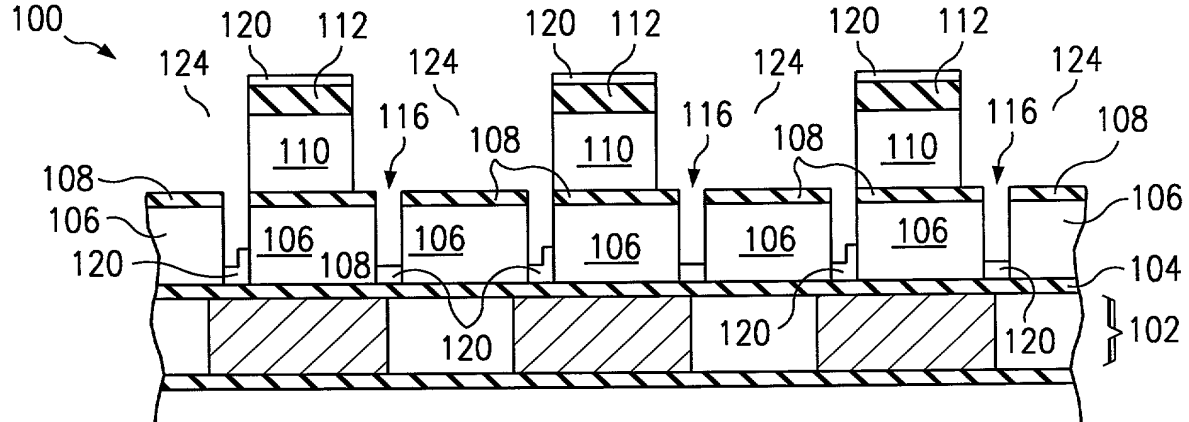

FIG. 2H

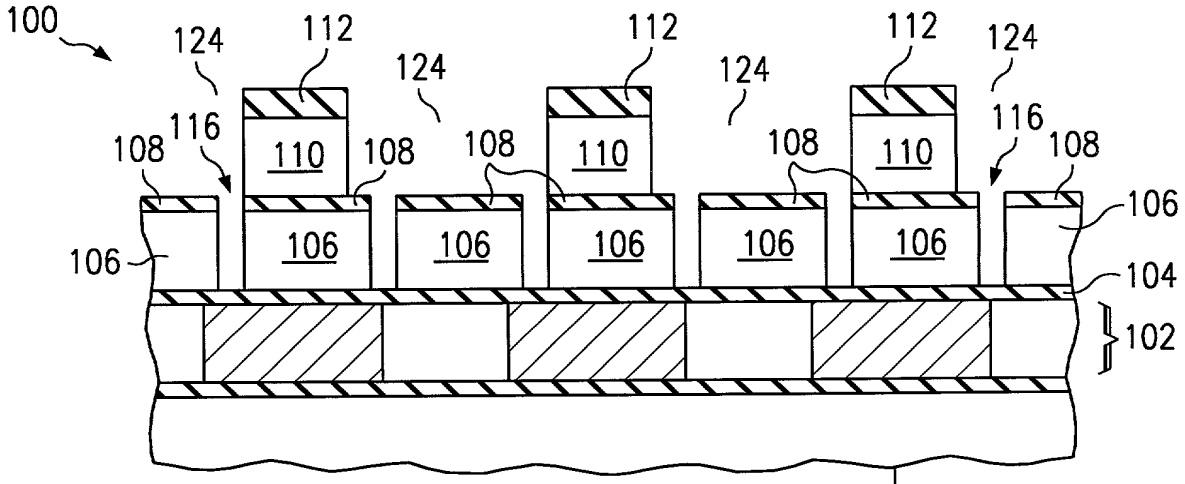

FIG. 2I

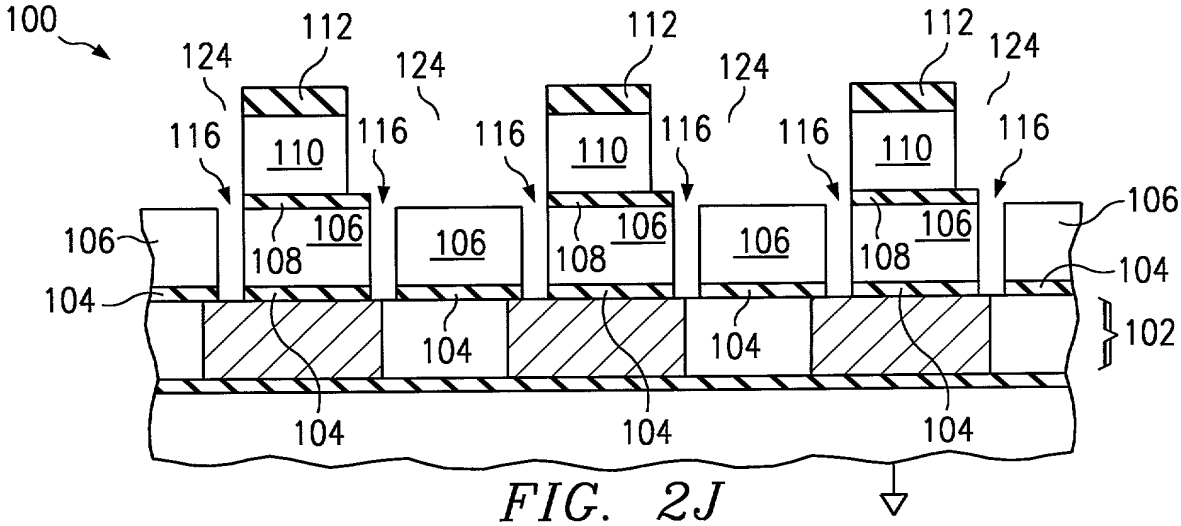

FIG. 2J

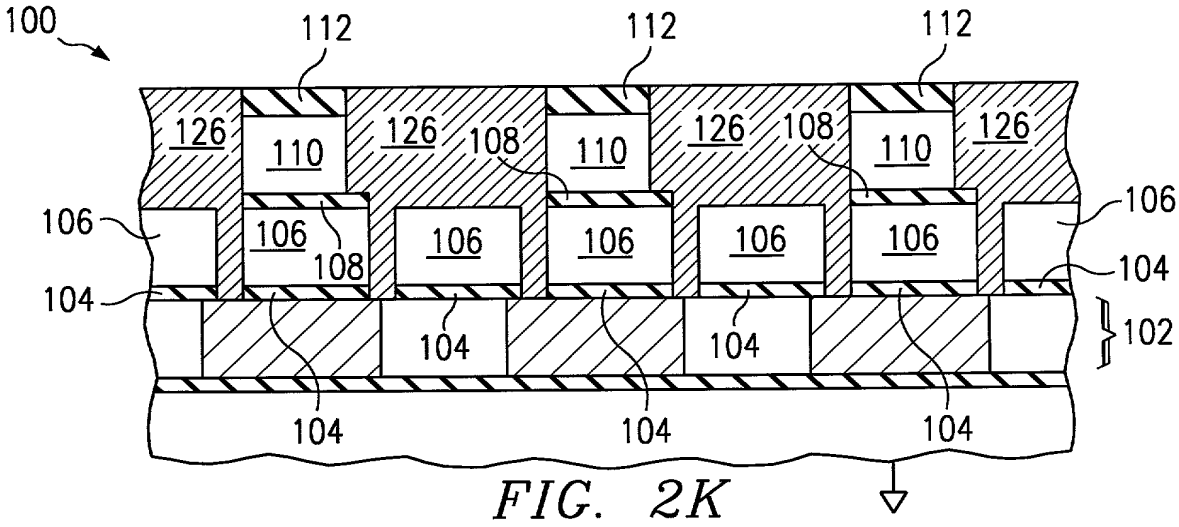

FIG. 2K

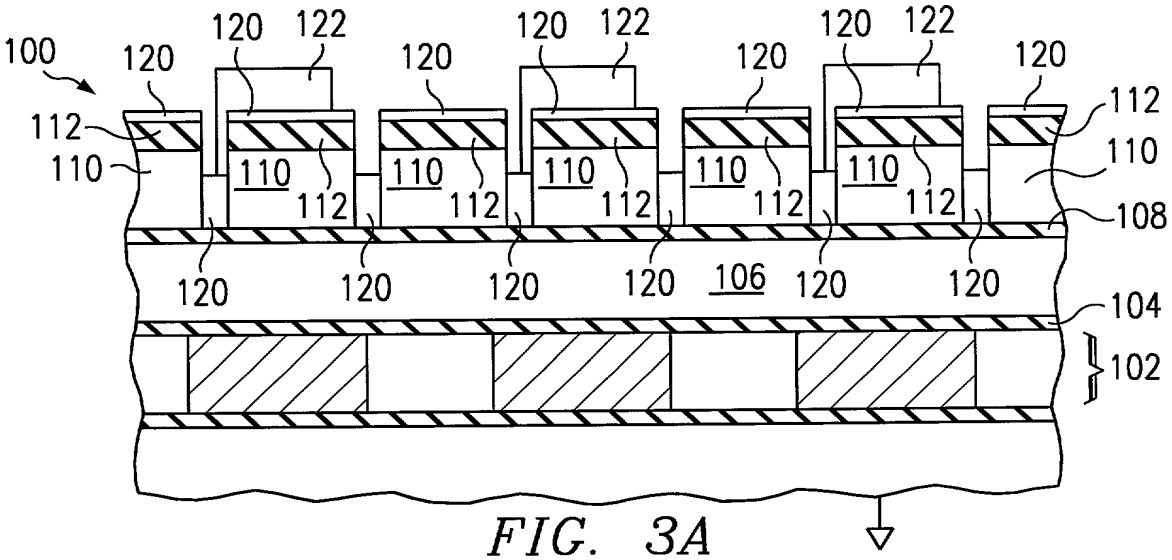
100
120
122
112
110
108
106
104
102

FIG. 3A

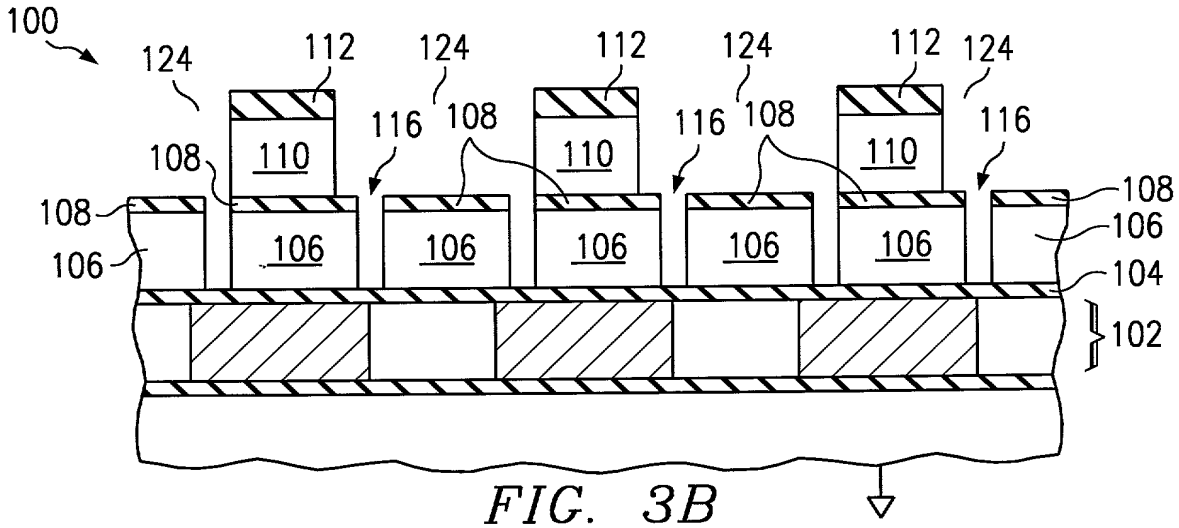
100
124
112
116
108
110
106
104
102

FIG. 3B

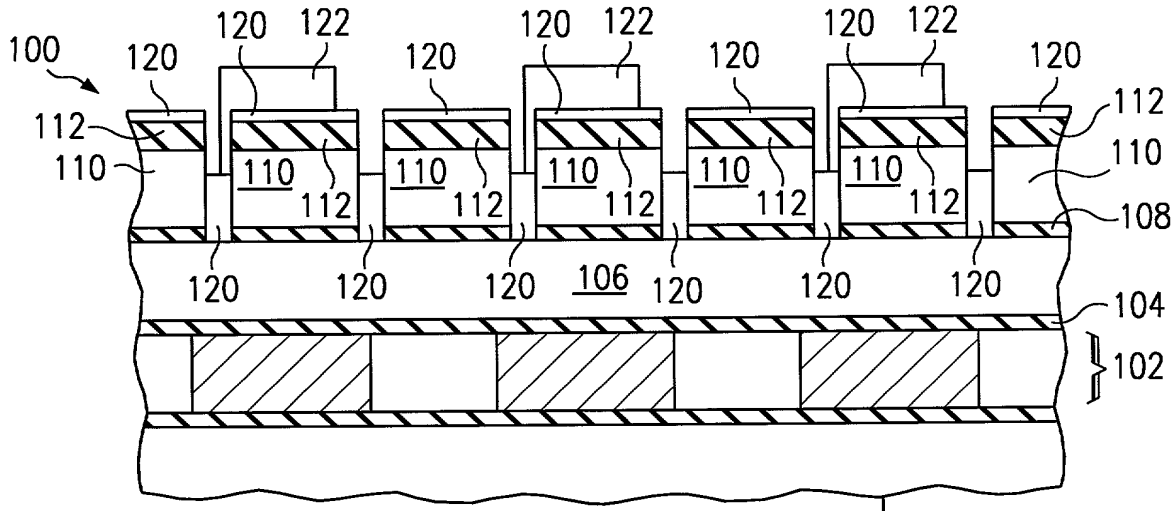

FIG. 4A

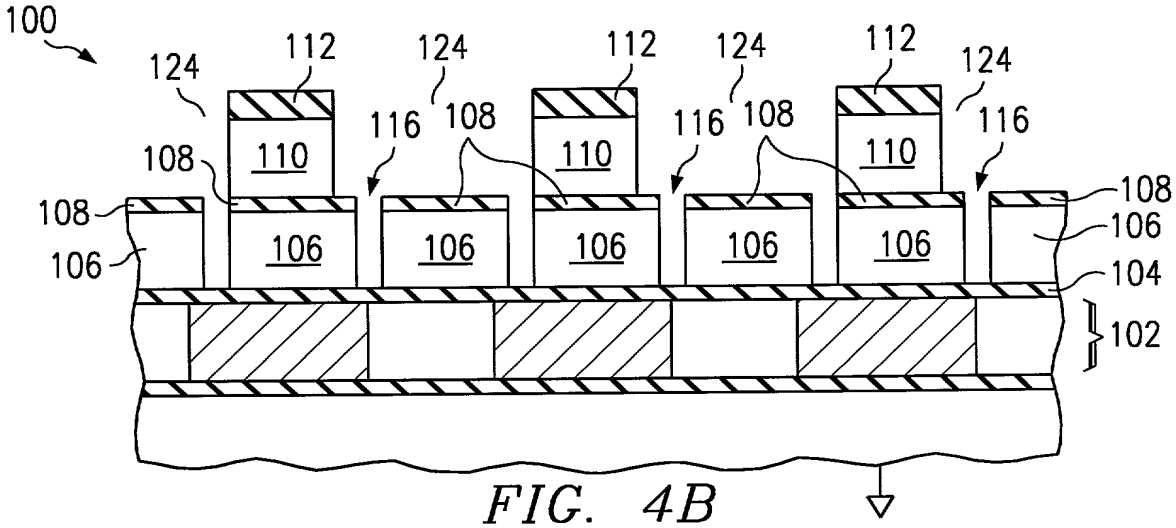

FIG. 4B

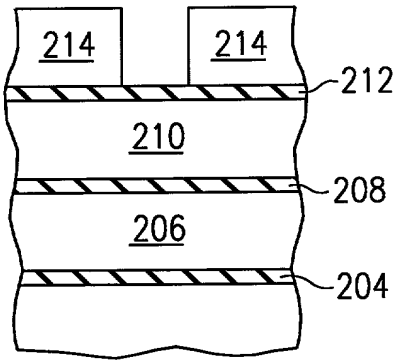

FIG. 5

ATTORNEY'S DOCKET NO.
TI-29276

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

PROCESS FLOW FOR DUAL DAMESCENE INTERCONNECT STRUCTURES

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

Jacqueline J. Garner, Reg. No. 36,144; Wade James Brady III, Reg. No. 32,080;
Mark A. Valetti, Reg. No. 36,707; Carlton H. Hoel, Reg. No. 29,934;
William B. Kempler, Reg. No. 28,288; Richard L. Donaldson, Reg. No. 25,673.

SEND CORRESPONDENCE TO:	DIRECT TELEPHONE CALLS TO:
Jacqueline J. Garner Texas Instruments Incorporated P.O. Box 655474, M/S 3999 Dallas, TX 75265	Jacqueline J. Garner (972) 278-9694 or (972) 917-4437

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SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE: 3/29/00	DATE: 3/30/00	DATE: 3/30/00

ATTORNEY'S DOCKET NO.
TI-29276

APPLICATION FOR UNITED STATES PATENT DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

PROCESS FLOW FOR DUAL DAMESCENE INTERCONNECT STRUCTURES

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

Jacqueline J. Garner, Reg. No. 36,144; Wade James Brady III, Reg. No. 32,080;
Mark A. Valetti, Reg. No. 36,707; Carlton H. Hoel, Reg. No. 29,934;
William B. Kempler, Reg. No. 28,288; Richard L. Donaldson, Reg. No. 25,673.

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SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE: 4/5/00	DATE: 4/11/2000	DATE: 3/30/00

ATTORNEY'S DOCKET NO.
TI-29276

APPLICATION FOR UNITED STATES PATENT DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56;

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SIGNATURE OF INVENTOR: Robert Kraft	SIGNATURE OF INVENTOR: Jeff West	SIGNATURE OF INVENTOR:
DATE: 3/30/00	DATE: 4-5-00	DATE: